AMENDMENTS TO THE SPECIFICATION

Replace the paragraph beginning on page 8, line 22, with the following:

Fast searcher 120a includes a memory block 216a coupled in parallel to multiple computation circuits 204-1 through 204-N. Each of the multiple computation circuits, e.g., 204-1 through 204-N, have an offset coupling arrangement with memory block 216a. For example, computation circuit 204-2 has a coupling arrangement to memory 216a that is offset from the coupling arrangement of computation circuit 204-1 by an offset A 214-1. Similarly, computation circuit N-1 204-N-1 is offset from computation circuit 204-2 by an offset B 214-2; and computation circuit N 204-N is offset from computation circuit 204-N-1 by offset ~~X~~ N 214-N. Offsets 214-1 through 214-N, between computation circuits 204-1 through 204-N, enable parallel correlation with unique phase offsets between an internally generated code sequence 210, input to and stored in memory block 216a, and a code sequence of a received input signal 208, input to and stored in each of computation circuits. Thus, a relative offset in the code sequence between each of the computing circuits 204-1 through 204-N is accomplished. In one embodiment, offsets between computation circuits are 512 chips for an IS-95 protocol separating base station pilot signals by a phase offset of 512 chips. Code sequence 210 is provided by code generator 113 of Figure 1 in the present embodiment. However, code sequence can be stored in, and provided by, a memory block in another embodiment. In contrast, input signal 208 is provided via antennae 101 and front-end processing block 103 of Figure 1.

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Replace the paragraph beginning on page 9, line 17, with the following:

Memory block 216a, which is a first in first out (FIFO) configuration, has a quantity of individual memories, e.g., 202a-202g, that yield a memory block of size 207 in the present embodiment. Individual memories 202a-202g can be any type of memory device capable of storing a state, e.g., flip-flop registers, flash random access memory (RAM), etc. Size 207 is determined by summing the quantity of the multiple bit slices in one of the computation circuits, e.g., 204-1, plus the sum of the offsets for all the computation circuits, e.g., offsets 214-1 through 214-N. This relationship enables sufficient memory resources in memory 216a to provide a code sequence stored in memory 216a to the applicable one of multiple computation circuits 204-1 through 204-N. Each bit slice, e.g., 203a and 203d, in a computation circuit, e.g., 204-1, is coupled to a specific memory, e.g., 202a and 202d respectively, in the memory block-216a, for the present embodiment. Similarly memories 202b-202e are coupled to computing circuit ~~2 202-2~~2 204-2, while memories 202c-202f are coupled to computing circuit (N-1) 204-N-1, and memories 202d-202g are coupled to computing circuit N 204-N.

Replace the paragraph beginning on page 12, line 1, with the following:

Fast searcher 120c of Figure 2C provides a separate input for each of the multiple computation circuits 204-1 through 204-N. In particular, code sequence 210 and offset 1 code sequence 210-1 through offset code sequence N 210-N, which are provided to computation circuits 204-1 through 204-N respectively, already have a unique code offset with respect to each other. Thus, no memory buffer is required for coupling input signals to computation circuits, as shown in Figure 213, nor is a long memory block 216a of Figure 2A.